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Serial number 09/247,974

AMENDMENTS

IN THE CLAIMSPlease amend the claims as follows.

1. (Twice Amended) A method of filling gaps [in a plane of and] between a pattern of interconnect lines forming a wiring structure on a semiconductor substrate, said interconnect lines having a top surface further having sidewalls, comprising the steps of:

providing a semiconductor substrate said substrate having a surface;

creating a network of interconnect lines on said surface of said substrate whereby said interconnect lines are separated by holes having bottoms between said interconnect lines thereby leaving said surface of said substrate partially exposed over said bottoms of said holes between said interconnect lines;

depositing a first layer of dielectric having a surface over said interconnect lines wiring structure thereby including said exposed surface of said semiconductor substrate;

performing an etch back of said first layer of dielectric;

depositing a second layer of dielectric having a surface over said etched back first layer of dielectric;

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etching said second layer of dielectric thereby creating exposed portions of said first layer of dielectric; and

depositing a layer of oxide over said etched second layer of dielectric thereby including said exposed portions of said first layer of dielectric.

3. (Twice Amended) The method of claim 1 wherein said interconnect lines contain a lower layer of polysilicon and [a] an upper layer of silicon nitride (SiN) said wiring structure [to be] is applied during the SAC process.

16. (Twice Amended) A method of filling gaps [in the plane of and] between a pattern of interconnect lines forming a wiring structure on a semiconductor substrate, said interconnect lines having a top surface further having sidewalls, comprising the steps of:

providing a semiconductor substrate said substrate having a surface;

creating a network of interconnect lines on said surface of said substrate whereby said interconnect lines are separated by holes having bottoms between said interconnect lines thereby leaving said surface of said substrate partially exposed over said bottoms of said holes between said interconnect lines;

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depositing a first layer of dielectric having a surface over said interconnect lines wiring structure thereby including said exposed surface of said semiconductor substrate;

performing an etch back of said a first layer of dielectric wherein said etch back is performing a Buffered Oxide Etch thereby forming a layer of first dielectric on the bottom of said holes between said interconnect lines thereby further forming deposits of said first dielectric on the top surfaces of interconnect lines said deposits partially overlaying the top surfaces of said interconnect lines thereby creating exposed top corners of said interconnect lines said top corners being located at intersects between said sidewalls of said interconnect lines and said top surface of said interconnect lines;

depositing a second layer of dielectric said deposition covering said layer of first dielectric on the bottom of said holes between said interconnect lines thereby further covering said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore covering the partially exposed top corners of said interconnect lines;

etching said second layer of dielectric to remove said second layer of dielectric in its totality except where said second layer of dielectric forms spacers on the sidewalls of said interconnect lines; and

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depositing a layer of PE-oxide or PE-TEOS over said spacers on the sidewalls of said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said layer of first dielectric on the bottom of the holes between said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over said first dielectric partially overlaying the top surfaces of said interconnect lines thereby furthermore depositing a layer of PE-oxide or PE-TEOS over the partially exposed top corners of said interconnect lines.

18. (Twice Amended) The method of claim 16 wherein said interconnect lines contain a lower layer of polysilicon and a upper layer of silicon nitride (SiN) said interconnect lines [to be] is applied during the SAC process.

REMARKS

Examiner B. Tran is thanked for his thorough examination of the Prior Art. Applicant has amended all claims as kindly suggested by the Examiner.

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.